REMARKS

Examiner Doan is thanked for her thorough examination of the Subject Patent Application. Amendments have been made to the Claims and is so doing are believed to now render this application in condition for allowance.

Regarding the rejections of Claims 1 - 10, as well as Claims 11 -19, under 35 USC 112, Examiner's kind suggestions have been employed in the currently amended Claims. Regarding Claim 1, line 11, the erroneous "second" wafer has been amended to "first' wafer. Regarding Claim 19, line 9, the erroneous "with or without an insulator layer between" has been amended to "with an insulator layer between". Therefore reconsideration of the rejected Claims under 35 USC 112, is requested. In addition the informalities in lines 7, and 15, of Claim 11, have been amended, replacing the incorrect "the said" to "said".

Regarding the rejections of Claims 1 - 19, under 35 USC 102, as anticipated by Godbey et al (US 5,013,681), this prior art attains the desired configuration of Si on insulator by etching or polishing thick layer 20, as well as layer 22, to expose Si layer 24. This is clearly described cols 3 -4, and in Figs. 1 - 6. The third embodiment of this prior art which Examiner cites, shown in Figs 9 - 13, again results in a silicon layer 74, on an underlying insulator layer, but again using the identical processing conditions, (such as etching or polishing), used in their first embodiment again shown using Figs. 1 - 6. This is stated in col 5, line 49 - 50. In direct contrast applicant's process describes and claims the desired configuration of silicon on an insulator layer via a **cleaving procedure**, a procedure that takes advantage of the stress and strain

gradient between the silicon and silicon alloy layer, allowing the novel cleaving procedure to be employed. Surely this is a different process than the process described in the Godbey prior art.

Regarding the rejection of the Claims 1- 19, under 35 USC 102, as anticipated by Sakaguchi et al (US 6,221,738), this prior art needs to convert both the silicon layer and the underlying silicon alloy layer to porous layers, then re-convert the porous silicon layer to a non-porous layer, now overlying a still porous silicon alloy layer, and then finally mechanically separating the non-porous silicon - porous silicon alloy interface. Again this complex process sequence is different from applicant's process in which a strain or stress gradient between a strained silicon layer and an underlying relaxed silicon alloy layer allows a **cleaving procedure** to perform the desired separation **without** having to convert and than reconvert the critical silicon layer to a porous and then a non-porous layer. Since this strained silicon layer in applicant's invention will be the layer in which the MOSFET device is formed in, it would be dangerous to continually change the density (porosity) of this layer. Therefore, again applicant's invention simplifies the attainment of a stained silicon layer on insulator via a **cleaving** procedure applied to an interface featuring **a strain gradient.**

Applicant has clearly described in independent Claims 1 and 11, the cleaving procedure performed at the silicon - silicon alloy interface, needing no extra process sequences such as polishing, etching or porosity changes, as described in the Godbey and Sakaguchi prior arts. Therefore reconsideration of the rejections of independent Claims 1 and 11, under 35 USC 102, based on the above arguments is requested.

Referring to the rejection of the Claims under 35 USC 103, as being unpatentable over Godbey et al (US 5,013,681), Sharma et al (US 5,344,524), in view of King et al (US4,142,925), not one of these prior art describe the attainment of a strained silicon layer on an underlying relaxed silicon alloy layer via a **cleaving procedure** applied to an interface featuring a strain gradient which allows the unique cleaving procedure to be successful. Therefore if none of these prior art describe this novel procedure no combination of the above prior art can result in applicant's invention. Therefore reconsideration of the rejections of independent Claims 1 and 11, and of dependent Claims 2 - 10, and 12 - 19, under 35 USC 103, is requested.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached page is captioned.

"Version with markings to show changes made"

It is requested that should Examiner Doan not find that the Claims are now Allowable that she call the undersigned attorney at 845-452-5863, to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg # 37,761

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

PLEASE AMEND THE CLAIMS AS FOLLOWS:

Claim 1. (currently amended) A method of forming a strained semiconductor layer, comprising the steps of:

providing a first wafer with a surface comprising of a first semiconductor layer of a first natural lattice constant;

forming a second semiconductor layer with a second natural lattice constant on the first semiconductor layer;

providing a second wafer with a surface with or without an insulator layer;

bonding said second semiconductor layer on said surface of said second wafer, resulting in a third wafer comprised of said second wafer, said second semiconductor layer, and said first wafer; and

performing a cleaving procedure so that said second semiconductor is separated from said first semiconductor layer and said ~~second~~ first wafer.

Claim 2. (original) The method of claim 1, wherein said second wafer is a single crystalline silicon substrate.

Claim 3. (original) The method of claim 1, wherein said second wafer is a single crystalline silicon substrate with an overlying insulator layer formed on it.

Claim 4. (original) The method of claim 3, wherein said insulator layer is a silicon dioxide layer.

Claim 5. (original) The method of claim 3, wherein said insulator layer is a silicon nitride layer.

Claim 6. (original) The method of claim 1, wherein said first semiconductor layer has a lattice constant greater than that of overlying said second semiconductor layer.

Claim 7. (original) The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising silicon and germanium.

Claim 8. (original) The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising of silicon and germanium, epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

Claim 9. (original) The method of claim 1, wherein said second semiconductor alloy layer is a silicon layer under tensile strain.

Claim 10. (original) The method of claim 1, wherein said second semiconductor layer is a silicon layer, epitaxially grown to a thickness between about 20 to 1000 Angstroms.